Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	ATTY. DKT. NO. 5500-79600 APPLICANT: Mitchell Alsup FILING DATE: July 8, 2003	SERIAL NO. 10/615,507 GROUP: 2186

U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

HD	A1	Yuan Chou, et al., "Instruction Path Coprocessors," March 2000, pp. 1-24.
	A2	Friendly, et al., "Putting the Fill Unit to Work: Dynamic Organizations for Trace Cache Microprocessors," Dept. of Electrical Engineering and Computer Sciences, The Univ. of Michigan, December 1998, 9 pages.
	A3	Bryan Black, et al., "Turboscalar: A High Frequency High IPC Microarchitecture," Dept. of Electrical and Computer Engineering, Carnegie Mellon Univ., June 2000, pp. 1-
	A4	Rotenberg, et al., "Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching," April 11, 1996, pp. 1-48.
	A5	Merten, et al., "An Architectural Framework for Run-Time Optimization," June 2001, pp. 1-43.
	A6	Jourdan, et al., "Increasing the Instruction-Level Parallelism through Data-Flow Manipulation," Intel, 11 pages.

EXAMINER: Hien T. Nguyen DATE CONSIDERED: 8/6/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.